Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**170 mils**

**GATE**

**SOURCE**

**192 mils**

**CHIP BACK IS DRAIN**

**Top Material: Al**

**Backside Material: CrNiAg**

**Bond Pad Size: S = .060” X .042” G = .025” X .018”**

**Backside Potential: Drain**

**Geometry: HEX-4 100V GEN III**

**APPROVED BY: DK DIE SIZE .170” X .192” DATE: 9/22/21**

**MFG: IR THICKNESS .016” P/N: IRFC9140**

**DG 10.1.2**

#### Rev B, 7/19/02